CLAIMS

What is claimed is:

1. A method comprising:

receiving circuit analysis results;

identifying a duplicate circuit analysis result among the received circuit analysis results; and

outputting a list of circuit analysis results that excludes the duplicate circuit analysis result.

2. The method of claim 1, further comprising:

sorting the circuit analysis results.

3. The method of claim 2, wherein the circuit analysis results are sorted alphabetically.

4. The method of claim 2, further comprising:

comparing each of the circuit analysis results with an adjacent circuit analysis result.

5. The method of claim 2, wherein the circuit analysis results are sorted based on types of circuit analysis results.

6. The method of claim 5, wherein the types of circuit analysis results comprise a type of result configured to enable detection of latch design defects.

7. The method of claim 5, wherein the types of circuit analysis results comprise a type of result configured to enable detection of dynamic gate design defects.

8. The method of claim 5, wherein the types of circuit analysis results comprise a type of result configured to enable detection of clock design defects.

9. The method of claim 5, wherein the types of circuit analysis results comprise a type of result configured to enable detection of pseudo-NMOS gate design defects.

10. The method of claim 5, wherein the types of circuit analysis results comprise a type of result configured to enable detection of pass-FET design defects.

11. A system comprising:

memory configured to store program code; and

at least one processor that is programmed by the program code to:

identify a duplicate circuit analysis result; and

output a list of circuit analysis results that excludes the duplicate circuit analysis result.

12. The system of claim 11, wherein the at least one processor is further programmed to sort the circuit analysis results.

13. The system of claim 12, wherein the circuit analysis results are sorted alphabetically.

14. The system of claim 12, wherein the at least one processor is further programmed to compare each of the circuit analysis results with an adjacent circuit analysis result.

15. The system of claim 12, wherein the circuit analysis results are sorted based on types of circuit analysis results.

16. The system of claim 15, wherein the types of circuit analysis results comprise a type of result configured to enable detection of latch design defects.

17. The system of claim 15, wherein the types of circuit analysis results comprise a type of result configured to enable detection of dynamic gate design defects.

18. The system of claim 15, wherein the types of circuit analysis results comprise a type of result configured to enable detection of clock design defects.

19. The system of claim 15, wherein the types of circuit analysis results comprise a type of result configured to enable detection of pseudo-NMOS gate design defects.

20. The system of claim 15, wherein the types of circuit analysis results comprise a type of result configured to enable detection of pass-FET design defects.

21. A computer readable medium having computer-readable instructions configured to:

receive circuit analysis results;

identify a duplicate circuit analysis result among the received circuit analysis results; and

output a list of circuit analysis results that excludes the duplicate circuit analysis result.

22. The computer readable medium of claim 1, wherein the computer-readable instructions are further configured to:

sort the circuit analysis results; and

compare each of the circuit analysis results with an adjacent circuit analysis result.

23. A system comprising:

means for receiving circuit analysis results;

means for identifying a duplicate circuit analysis result among the received circuit analysis results; and

means for outputting a list of circuit analysis results that excludes the duplicate circuit analysis result.

24. The system of claim 23, further comprising:

means for sorting the circuit analysis results; and

means for comparing each of the circuit analysis results with an adjacent circuit analysis result.